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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,543	08/05/2003	Katuhiro Kanauchi	030915	6426

38834 7590 10/18/2005

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,543	KANAUCHI, KATUHIRO	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-23-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: DEVICE FOR AND METHOD OF APPLYING A REVERSE BIASED VOLTAGE TO A LUMINESCENT DISPLAY PANEL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuda (US 6,380,689) in view of Inukai (US 2002/0180671).

With respect to claim 1, Okuda discloses, a device for driving a luminescent display panel, the device being the one for driving an active matrix type display panel (col. 3, lines 25-30) that is equipped with a plurality of luminescent elements (col. 3, lines 25-30) that are arrayed at the positions of intersection between a plurality of data lines (B1... Bn in fig. 2) and a plurality of scanning lines (A1 ... Am in fig. 2) and at least each one of that is luminescence controlled via a light-up drive transistor (47 in fig. 11),

Having a construction wherein a light-up mode in which a forward-directional voltage (-Ve in fig. 11) is applied to the luminescent element via the light-up drive

transistor and a reverse bias voltage applying mode in which a reverse bias voltage (Va in fig. 11) is applied to the luminescent element via the light-up drive transistor can be selectively determined (col. 5, line 56; also note 28c in fig. 11).

Okuda does not expressly disclose, wherein, in case where the reverse bias voltage applying mode is selected, there operates reverse bias voltage applying means that applies a reverse bias voltage to the luminescent element while bypassing the light-up drive transistor.

Inukai discloses the inclusion of either a transistor or a diode (104 in fig. 1a and 109 in fig. 17) to bypass the light-up drive transistor (102 in figs. 1a and 17) when applying a reverse bias to the luminescent element (para. 36).

Okuda and Inukai are analogous art because they are from the same field of endeavor namely OLED reverse bias pixel driving circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the pixel circuit of Okuda with the rectifying pixel circuit of Inukai.

The motivation for doing so would have been to prevent reduction in luminance of the organic element and to improve the overall quality of the display (Inukai, last three lines of para. 29).

Therefore, it would have been obvious to combine Inukai with Okuda for the benefit of no concern of the state of the drive transistor to obtain the invention as specified in claim 1.

With respect to claim 2, Okuda and Inukai disclose, the device for driving a luminescent display panel, according to claim 1 (see above).

Inukai further discloses, wherein the reverse bias voltage applying means include a diode or TFT (104 in fig. 1a and 109 in fig. 17) that, by being connected in parallel to the light-up drive transistor, becomes electrically conductive when applied with a reverse bias voltage (note para. 36).

Therefore it would have been obvious to combine Inukai with Okuda for the reasons mentioned above in claim 1 to obtain the invention as specified in claim 2.

With respect to claim 3 (both; dependent on claim 2 (3/2) and solely dependent upon claim 1 (3/1)), Okuda and Inukai disclose, the device for driving a luminescent display panel according to claim 1 or 2 (see above).

Okuda further discloses, wherein electrode lines (C in fig. 11) having commonly connected thereto the plurality of luminescent elements arrayed correspondingly to the scanning lines (Ai in fig. 11) are formed in the way of their being electrically separated every scanning line (note fig. 11 and 10), whereby the device has a construction wherein, by applying a prescribed voltage level to the respective electrode lines, the reverse bias voltage applying mode is selected (note col. 5, lines 56-62).

With respect to claim 4/3/2 and 4/3/1, Okuda and Inukai disclose, the device for driving a luminescent display panel, according to claim 3 (see above).

Okuda further discloses, wherein the electrode lines are cathode lines having commonly connected thereto the cathode sides of the respective luminescent elements

arrayed correspondingly to the scanning lines (note figure 11 having the cathode connected to the electrode line C).

With respect to claim 5/3/2 and 5/3/1, Okuda and Inukai disclose, the device for driving a luminescent display panel, according to claim 3 (see above).

Okuda further discloses wherein the electrode lines are anode lines having commonly connected thereto the anode sides of the respective luminescent elements arrayed correspondingly to the scanning lines (note figure 10 having the anode connected to electrode line C).

With respect to claims 6-8, Okuda and Inukai disclose luminescent panels according to claims 1, 2, 3/1, 3/2/1, 5/3/2/1 and 5/3/1 (see above).

Okuda further discloses, the luminescent element being constructed of organic materials (col. 1, lines 19-20 and col. 3, lines 31-34).

4. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuda (US 6,380,689) in view of Yamazaki (US 6,777,249).

With respect to claim 9, Okuda discloses, the method of driving an active matrix type display panel (col. 3, lines 25-30) that is equipped with a plurality of luminescent elements that are arrayed at the positions of intersection between a plurality of data lines and a plurality of scanning lines and at least each one of that is luminescence controlled via a light-up drive transistor (note figures 2 and 11),

comprising a luminescent element light-up step of applying a forward-directional voltage to the luminescent element via the light-up drive transistor and a reverse bias voltage applying step of applying a reverse bias voltage to the luminescent element via

the light-up drive transistor (col. 9, lines 1-22, which discusses applying both a forward and reverse bias to the element).

Okuda does not expressly disclose, whereby, in case where the reverse bias voltage applying step is executed, there operates reverse bias voltage applying means that applies a reverse bias voltage to the luminescent element while bypassing the light-up drive transistor.

Yamazaki discloses the inclusion of a transistor (408 in fig. 7) to bypass the light-up drive transistor (402 in fig. 7) when applying a reverse bias to the luminescent element (also note col. 15, lines 31-47, which discusses the application of the reverse bias).

Okuda and Yamazaki are analogous art because they are directed to a similar problem solving area, applying a reverse biasing voltage to an OLED panel.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the panel circuitry of Okuda with the rectifying pixel circuitry of Yamazaki.

The motivation for doing so would have been to allow actively select which pixel to apply the reverse biasing to without selecting all of the pixels at once (Yamazaki, col. 15, lines 34-37 and lines 48-50).

Therefore, it would have been obvious to combine Yamazaki with Okuda for the benefit of not requiring the gate and light-up transistor to be powered to obtain the invention as specified in claim 9.

With respect to claim 10, Okuda and Yamazaki disclose, the method of driving a luminescent display panel according to claim 9 (see above).

Yamazaki further discloses, wherein electrode lines having commonly connected thereto the plurality of luminescent elements arrayed correspondingly to the scanning lines are formed in the way of their being electrically separated every scanning line (note the opposing electrode lines attached to 407 in fig. 8a, these lines are arrayed correspondingly to the scanning lines, G1-y), whereby a reverse bias voltage is applied in the way in which the timings of applying it do not coincide with each other ever electrode line (col. 15, lines 48-50, discloses that the reverse bias may be performed line by line at different timings).

With respect to claim 11, Okuda and Yamazaki disclose, the method of driving a luminescent display panel, according to claim 10 (see above).

Okuda further discloses, wherein a unit frame period is divided into a plurality of sub-field (note fig. 4), multi-gradation expression is executed (col. 4, lines 2-3); and within the non-luminescing time period of the luminescent element in the sub-field period, a reverse bias voltage is applied (col. 9, lines 7-10, disclose the application of the reverse bias voltage during the addressing period, a non-luminescing period).

With respect to claim 12, Okuda and Yamazaki disclose, the method of driving a luminescent display panel, according to claim 10 (see above).

Okuda further discloses wherein, within an addressing period of time wherein addressing is done every scanning line; a reverse bias voltage is applied to the electrode line (col. 9, lines 7-10).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Howard et al. (US 6,023,259) discloses a pixel structure comprising a rectifying diode to bypass the drive transistor when applying reverse bias voltages in figure 1.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 8:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
10-4-05

REGINA LIANG
PRIMARY EXAMINER